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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,327	09/28/2001	Alaa F. Alani	A2-4059 1496.00150	3179

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LSI LOGIC CORPORATION
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PATENT LAW DEPARTMENT
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EXAMINER	
DAMIANO, ANNE L	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,327	ALANI ET AL.	
	Examiner	Art Unit	
	Anne L Damiano	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Pages 4-6 and 12 make reference to figures 2A-F. However, no such figures are present. Either such drawings much be added or such references must be removed from the specification.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities: Line 6-7, "present said signals received from said circuit on a transmission bus," specifically, "said signals received from circuit" lacks antecedent basis. The claim does not include the step of the buffers receiving

the signals from the circuit. Therefore, for purpose of a prior art rejection, this is interpreted as rather as saying, "present said signals on a transmission bus." Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Schenck (6,072,329).

As in claim 1, Schenck discloses an apparatus comprising:

A circuit configured to (i) monitor a plurality of signals for transitions and (ii) invert said signals (transmit in complementary state) when at least a predetermined number of said signals (more than half of the data lines) transition in a predetermined direction (column 2: lines 16-30); and

A plurality of buffers configured to present said signals received from said circuit on a transmission bus (column 2: lines 28-30).

As in claim 2, Schenck discloses the apparatus according to claim 1, wherein said circuit is further configured to invert (transmit in complementary state) said signals when at least said predetermined number of said signals transition in an opposite direction of said predetermined direction (column 2: lines 18-22). (The system determine if more than half of the signals transition from both high to low and low to high.)

As in claim 3, Schenck discloses the apparatus according to claim 1, wherein said predetermined number is greater than one half of a total number of said signals (column 2: lines 22-24).

As in claim 4, Schenck discloses the apparatus according to claim 1, wherein said circuit comprises: a transition checker circuit configured to present a plurality of transition signals each indicating a transition direction of one of said signals;

A control circuit configured to present a flag signal (parity signals) when at least said predetermined number of said transition signals have said predetermined direction; and

An inverter circuit configured to invert said signals in response to said flag signal (column 4: lines 7-23). (When the parity signal is a 1, data bits will be transmitted in the opposite direction from which it was received. Therefore, the parity signals are acting as flags that cause signals to be inverted.)

As in claim 5, Schenck discloses the apparatus according to claim 4, wherein said buffers are further configured to present said flag signal on said transmission bus (column 4: lines 45-53).

As in claim 6, Schenck discloses the apparatus according to claim 4, wherein said transition checker circuit comprises:

A plurality of flip-flops configured to present said signals as a plurality of sampled signals;

A plurality of inverters configured to present said signals as a plurality of inverted signals; and

A plurality of logic gates configured to present said transition signals in response to said sampled signals and said inverted signals (column 4: lines 1-6).

As in claim 7, Schenck discloses the apparatus according to claim 4, wherein said circuit further comprises a plurality of flip-flops configured to store said signals as presented by said inverter circuit (column 4: lines 33-37).

As in claim 8, Schenck discloses the apparatus according to claim 7, wherein said circuit further comprises a clock configured to present a clock signal to said flip-flops (column 4: lines 33-37).

As in claim 9, Schenck discloses the apparatus according to claim 8, wherein said buffers are further configured to present said flag signal on said transmission bus and said transition checker circuit comprises:

A plurality of flip-flops configured to present said signals as a plurality of sampled signals;

A plurality of inverters configured to present said signals as a plurality of inverted signals; and

A plurality of logical gates configured to present said transition signals in response to said sampled signals and said inverted signals (column 4: lines 1-23).

As in claim 10, Schenck discloses a method of reducing noise induced by transitions of a plurality of signals, the method comprising the steps of:

(A) monitoring said signals for said transitions;

(B) inverting said signals (transmit in complementary state) in response to at least a predetermined number (more than half of the data lines) of said signals transitioning in a predetermined direction (column 2: lines 16-30); and

(C) presenting said signals on a transmission bus (column 2: lines 28-30).

As in claim 11, Schenck discloses the method according to claim 10, further comprising the step of inverting said signals in response to at least said predetermined number of said signals transitioning in an opposite direction as said predetermined direction (column 2: lines 18-22).

(The system determine if more than half of the signals transition from both high to low and low to high.)

As in claim 12, Schenck discloses the method according to claim 10, wherein said predetermined number is greater than one half of a total number of said signals (column 2: lines 22-24).

As in claim 13, Schenck discloses the method according to claim 10, wherein step (A) comprises the sub-steps of:

Generating a plurality of transition signals each indicating a transition direction of one of said signals; and

Generating a flag signal (parity signals) when at least said predetermined number of said transition signals have said predetermined direction (column 4: lines 7-23). (When the parity signal is a 1, data bits will be transmitted in the opposite direction from which it was received. Therefore, the parity signals are acting as flags that cause signals to be inverted.)

As in claim 14, Schenck discloses the method according to claim 13, further comprising the step of presenting said flag signal on said transmission bus (column 4: lines 45-53).

As in claim 15, Schenck discloses the method according to claim 13, wherein presenting said plurality of transition signals comprises the sub-steps of:

Sampling said signals to present a plurality of sampled signals;

Inverting said signals to present a plurality of inverted signals; and

Logically combining said sampled signals and said inverted signals to present said transition signals (column 4: lines 1-6).

As in claim 16, Schenck discloses the method according to claim 13, further comprising the step of storing said signals prior to presenting said signal on said transmission bus (column 4: lines 33-37).

As in claim 17, Schenck discloses the method according to claim 16, further comprising the step of generating a clock signal to control said storing (column 4: lines 33-37).

As in claim 18, Schenck discloses an integrated circuit comprising:

Means for monitoring a plurality of signals for transitions;

Means for inverting said signals in response to at least a predetermined number of said signals transitioning in a predetermined direction; and

Means for presenting said signals on a transmission bus (column 4: lines 1-23).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. After approximately October 15th, the examiner can be reached at (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER